UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,344	04/15/2004	Hiroyuki Kanda	2004_0586A	6329

513 7590 02/28/2007

WENDEROTH, LIND & PONACK, L.L.P.
2033 K STREET N. W.
SUITE 800
WASHINGTON, DC 20006-1021

EXAMINER	
PATEL, TAYAN B	
ART UNIT	PAPER NUMBER
1709	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/28/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

B/

Office Action Summary	Application No.	Applicant(s)	
	10/824,344	KANDA ET AL.	
	Examiner	Art Unit	
	Tayan B. Patel	1709	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/09/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2,3, 4, 5, 6, 7, 8, 15, 16, 17, 18, 19, 21, and 22 of the present invention are rejected under 35 U.S.C. 102(b) as being anticipated by Basol et al. (US 6,943,112).

As to claim 1, Basol et al. discloses a plating method that prepares a substrate having relatively narrow recesses and a relatively broad recess defined in a surface (See Column 6, lines 24-30; See also Figure 2). Moreover, Basol et al. discloses a first plating under plating conditions for filling a metal in said narrow recess (See Column 5, 35-56; See also Figure 2). In addition, Basol et al. discloses a second plating under plating conditions for filling a metal in said broad recess (See Column 56, lines 57-67; See also Figure 2).

As to claim 2, Basol et al. discloses a method wherein the entire surface of said narrow recess and said broad recess are fully covered with a seed layer. See Column 1, lines 34-37.

As to claim 3, Basol et al. discloses a method wherein said first plating is performed under plating conditions for a relatively high bottom-up capability, and said second plating is performed under plating conditions for a relatively high leveling capability. See Column 9, lines 14-26.

As to claim 4, Basol et al. discloses a narrow recess with a width less than 0.2 micrometers and said broad recess has a width of 0.2 micrometers or greater. See Column 2, lines 31-37.

As to claim 5, Basol et al. discloses a substrate having a plurality of narrow recesses defined in the surface thereof. See Column 5, lines 35-37; See also Figure 1B.

As to claim 6, Basol et al. discloses a substrate having a plurality of broad recesses defined in the surface thereof. See Column 2, lines 31-37; See also Figure 2.

As to claim 7, Basol et al. discloses a first plating and second plating performed under plating conditions including different current densities upon plating. See Column 8 lines 54-65; See also Column 9, lines 20-22.

As to claim 8, Basol et al. discloses a second plating process performed under plating conditions including a current density higher than said first plating. See Column 8, lines 54-65; See also Column 9, lines 20-22.

As to claim 15, Basol et al. disclose first and second plating performed using plating solution containing different additives added thereto. See column 9, lines 14-26.

As to claim 16, Basol et al. discloses an additive added to the plating solution in the first plating having a relatively high bottom-up capability, and the additive added to the plating solution used in the second plating having a relatively high leveling capability. See Column 9, lines 14-26.

As to claim 17, Basol et al. discloses plating solutions used in the first and second plating comprising a copper sulfate plating solution, and the plating solution used in the second plating having a less accelerator component and a more leveler component than the plating solution in the first plating. See Column 11, lines 23-62.

As to claim 18, Basol et al. discloses first and second plating performed using plating solutions having different compositions. See Column 11, lines 55-57.

As to claim 19, Basol et al. discloses a plating solution used in first plating and second plating comprising a copper sulfate solution (See Column 7, lines 7-12), and the plating solution used in said second plating has a lower copper concentration due to its sacrificial purpose and is optimized specifically for planar deposition (See Column 11, lines 19-56). One skilled in the art would understand the inversely proportional relationship between planar deposition and sulfuric acid concentration because the addition of levelers would lower the sulfuric acid concentration in the plating solution in comparison to the first plating process.

As to claim 21, Basol et al. discloses an additive added to a plating solution used in the first plating having a relatively high bottom-up capability and an additive added to

a plating solution used in the second plating having a relatively high leveling capability. See Column 9, lines 14-26. In addition, Basol et al discloses a current density in second plating greater than a current density in first plating. See Column 8, lines 54-65; See also Column 9, lines 20-22.

As to claim 22, Basol et al. discloses a plating solution used in first plating and second plating comprising a copper sulfate solution (See Column 7, lines 7-12), and the plating solution used in said second plating has a lower copper concentration due to its sacrificial purpose and is optimized specifically for planar deposition (See Column 11, lines 19-56). One skilled in the art would understand the inversely proportional relationship between planar deposition and sulfuric acid concentration because the addition of levelers would lower the sulfuric acid concentration in the plating solution in comparison to the first plating process. In addition, Basol et al. discloses current density in second plating is greater than a current density in first plating. See Column 8, lines 54-65; See also Column 9, lines 20-22.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 9 and 10 are rejected under 35 U.S.C 103(a) as being unpatentable over Basol et al. (US 6,943,112) and further in view of Nagai et al. (US 2002/0027081).

With respect to claim 9, Basol et al. discloses all of the claimed limitations as discussed with respect to claim 1, 7, and 8 above, yet fails to set the current density of first plating between 0.1 to 1.5 A/ dm^2, and a current density of second plating between 2 to 7 A/ dm^2.

Nagai et al. discloses an apparatus and method for plating a substrate with copper interconnects in order to fill recesses. In this reference, the first plating is performed at a current density between 0.1 to 1.5 A/dm^2 and the second plating is performed at a current density between 2 to 7 A/dm^2 in order to prevent the occurrence of burnt deposit and lower productivity. See Page 11, paragraph 0141; See also Page 9, paragraph 0124.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the current densities for the 2 plating steps in Nagai et al. in

Basol et al. in order to order to prevent the occurrence of burnt deposit and lower productivity. See Page 9, paragraph 0124.

With respect to claim 10, Nagai et al. further discloses a current density in second plating that increases more progressively than said first plating. See Page 11, paragraph 0141.

6. Claim 11, 12 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Basol et al. (US 6,943,112) and further in view of Mikkola et al. (US 2002/0074231).

With respect to claim 11, Basol et al. discloses all of the claimed limitation as discussed with respect to claim 1 above, but fails to disclose a second plating process performed at a higher plating rate than said first plating.

Mikkola et al. discloses a method of filling small recesses in a substrate. In this reference, the second plating process is taught to perform at a higher plating rate than said first plating process in order to reduce topography and thickness of the copper deposit produced. See Page, 3 paragraphs 27-28.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the higher second plating rate in the application of Mikkola et al. in Basol et al. in order to reduce the topography and thickness of the copper deposit produced. See Page 3, paragraphs 27-28.

With respect to claim 12, Basol et al. further discloses a first plating performed using a copper sulfate plating solution having a large proportion of an accelerator component (low acid version of plating chemistry may require different accelerator and

suppressor concentrations such as an accelerator concentration of about 4-8 ml/l, and suppressor concentration of 2-4 ml/l). See Column 7, lines 8-14.

With respect to claim 20, modified Basol et al. discloses all of the claimed limitations as discussed with respect to clam 1, yet fails to disclose a first plating and second plating performed under plating conditions including different relative speeds of the plating solution upon plating.

Mikkola et al. discloses a method of filling small recesses in a substrate. In this reference, the second plating process is taught to perform at a higher plating rate than said first plating process in order to reduce topography and thickness of the copper deposit produced. See Page, 3 paragraphs 27-28. Because speed is a function of the rate a plating solution is plated upon a substrate, this reference when combined with Basol et al. teaches all of the limitations of claim 20.

As such, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the higher second plating rate (speed a function of plating rate) in the application of Mikkola et al. in Basol et al. in order to reduce the topography and thickness of the copper deposit produced. See Page 3, paragraphs 27-28.

6. Claims 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Basol et al. (US 6,943,112) in light of Mikkola et al. (US 2002/0074231) and further in view of Dubin et al. (US 2002/0036145).

With respect to claim 13, modified Basol et al. disclose all of the structure as discussed with respect to claims 1, 11 and 12 above, yet fails to disclose an accelerator component comprising a sulfur-based organic compound.

Dubin et al. discloses a copper electroplating method in the fabrication of interconnect structures in semiconductor devices. Dubin et al. teaches an accelerating agent comprising sulfur-based organic compound in order to completely fill recesses as well as eliminate grain mismatch between a seed layer and contact. See Column 3, lines 21-31; See also Column 7, lines 1-6, 46-53.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the accelerating agent comprising a sulfur-based organic compound in Dubin et al. in Basol et al. in order to completely fill recesses as well as eliminate grain mismatch between a seed layer and contact. See Column 3, lines 21-31; See also Column 7, lines 1-6, 46-53.

7. Claim 14 is rejected under 35 U.S.C 103(a) as being unpatentable over Basol et al. (US 6,943,112) and further in view of Taylor et al. (US 6,309,528).

Basol et al. disclose all of the claimed limitations as discussed with respect to claim 1 above, yet fails to discloses that after first plating is performed, a reverse electric field is applied for a short period of time, and thereafter said plating is performed.

Taylor et al. discloses a method for electrodepositing metals onto a substrate having different transverse dimensions. In this reference, a reverse electric field (See Column 10, lines 14-19) is cycled after first plating (See Column 9, lines 50-60) and

before a second plating (See Column 10, lines 32-36) in order to completely fill the recesses or provide a conformal coating (See Column 10, lines 20-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a reverse electric field in Taylor et al. in Basol et al. in order to completely fill the recesses or provide a conformal coating. See Column 10, lines 20-27.

8. Claims 23, 24 and 25 are rejected under 35 U.S.C 103(a) as being unpatentable over Basol et al. (US 6,943,112) and further in view of Hongo et al. (US 7,033,463).

With respect to claim 23, Basol et al. discloses all of the claimed limitations as discussed with respect to claim 1 above, yet fails to disclose that before said first plating is performed, a voltage is applied between the substrate and an anode which has been in contact with a plating solution before the substrate is brought into contact with the plating solution, and the voltage remains applied and said substrate and said plating solution are brought into contact with each other.

Hongo et al. disclose a method and apparatus for plating recesses in semiconductor substrates. Hongo et al. teaches that before said first plating is performed, a voltage is applied between the substrate and an anode which has been in contact with a plating solution before the substrate is brought into contact with the plating solution, and the voltage remains applied and said substrate and said plating solution are brought into contact with each other in order to prevent the occurrence of a Cannizarro reaction and to achieve a plating process of high stable quality. See Column 15, lines 44-66; See also Column 13, lines 21-32.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply voltage between substrate and an anode in contact with a plating solution before first plating occurs and the voltage remains applied once the substrate and plating solution are in contact as discussed in Hongo et. al. in Basol et al. in order to prevent the occurrence of a Cannizarro reaction and to achieve a plating process of high stable quality. See Column 15, lines 44-66; See also Column 13, lines 21-32.

With respect to claim 24, Hongo et al. further discloses a voltage applied between the anode and substrate before the plating solution and substrate are brought into contact via a voltage control process to control voltage at a predetermined value. See Column 15, lines 44-66. In addition, the reference teaches a first plating performed with a current control process that controls the current flowing between the substrate and the anode at a predetermined value. See Column 16, lines 42-57.

With respect to claim 25, Hongo et al. further teaches a voltage applied between the anode and substrate before the plating solution and substrate are brought into contact via a voltage control process to control voltage at a predetermined value. See Column 15, liens 44-66. In addition, the reference teaches a first plating performed with a voltage control process that controls the voltage applied between said substrate and said anode at a predetermined value. See Column 16, lines 44-66.

9. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Basol et al. (US 6,943,112) and further in view of Kunisawa et al. (US 20020020627).

Basol et al. discloses all of the claimed limitations as discussed with respect to claim 1 above, yet fails to disclose that a first and second plating are performed by an impregnations plating process.

Kunisawa et al. discloses a method and apparatus for plating a substrate with copper by filing recesses. This reference teaches a plating process that includes a plating liquid impregnated material, 110, that is impregnated with the plating liquid to wet the surface of the anode, 98, in order to prevent a black film from falling onto the plated surface of the substrate by drying, and oxidizing as well as facilitating escape of air to the outside when the plating liquid is poured between the surface, to be plated, of the substrate and the anode. See Column 19, lines 34-60.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the impregnations plating process in Kunisawa et al. in order to prevent a black film from falling onto the plated surface of the substrate by drying, and oxidizing as well as facilitating escape of air to the outside when the plating liquid is poured between the surface, to be plated, of the substrate and the anode. See Column 19, lines 34-60.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tayan B. Patel whose telephone number is (571) 272-9806. The examiner can normally be reached on Monday-Thursday, 7:30-5:00 PM, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Neckel D. Alexa can be reached on (571) 272-9827. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

*****
TBP

ALEXA D. NECKEL
SUPERVISORY PATENT EXAMINER